SIGNAL FLOW DRIVEN CIRCUIT ANALYSIS AND PARTITION TECHNIQUE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to and the benefit of the filing date of provisional patent application Serial No. 60/442,306 filed Jan. 27, 2003.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to circuit analysis and partition and more specifically, it relates to a signal flow driven circuit analysis and partition technique for mixed-signal circuit performance optimization, yield enhancement and layout optimization.

2. Description of the Related Art

It can be appreciated that circuit analysis and partition have been in use for years. Typically, circuit analysis and partition are comprised of manual partition of circuit blocks based on their functionality and physical requirement during the circuit design and layout stages. For RF/Analog circuit blocks, identifying the critical signal flow is either not performed or implicitly identified at the layout stages manually by layout designers. Circuit optimization is commonly performed by trial-and-error with heavy-duty emulators like SPICE or Spectre.

The main problem with conventional circuit analysis and partition are that the mixed signal circuit designs often suffer sub-optimal block level partition or no partition at all due to lack of an automated solution. This results in either compromised performance of

the product or excessive physical area of the layout. Another problem with conventional circuit analysis and partition are that massive numerical simulations are needed in optimizing the performance of the circuit. Simulation can be prohibitively time and/or computation power intensive, that performance optimization may not be feasible for certain scale of circuits. Another problem with conventional circuit analysis and partition are that it is difficult to assure high quality layout, as it is up to the layout designer to manually identify the critical signal path during layout stage, which is largely dependent on designers' experience level and extremely error prone.

While these devices may be suitable for the particular purpose to which they address, they are not as suitable for mixed signal circuit performance optimization, yield enhancement and layout optimization. The main problem with conventional circuit analysis and partition are that the mixed signal circuit designs often suffer sub-optimal block level partition or no partition at all due to lack of an automated solution. This results in either compromised performance of the product or excessive physical area of the layout. Another problem is that massive numerical simulations are needed in optimizing the performance of the circuit. Simulation can be prohibitively time and/or computation power intensive, that performance optimization may not be feasible for certain scale of circuits. Also, another problem is that it is difficult to assure high quality layout, as it is upto the layout designer to manually identify the critical signal path during layout stage, which is largely dependent on designers' experience level and extremely error prone.

In these respects, the signal flow driven circuit analysis and partition technique according to the present invention substantially departs from the conventional concepts and designs of the prior art, and in so doing provides an apparatus primarily developed for the purpose of mixed signal circuit performance optimization, yield enhancement and layout optimization.

SUMMARY OF THE INVENTION

In view of the foregoing disadvantages inherent in the known types of circuit analysis and partition now present in the prior art, the present invention provides a new signal flow driven circuit analysis and partition technique construction wherein the same can be utilized for mixed signal circuit performance optimization, yield enhancement and layout optimization.

The general purpose of the present invention, which will be described subsequently in greater detail, is to provide a new signal flow driven circuit analysis and partition technique that has many of the advantages of the circuit analysis and partition mentioned heretofore and many novel features that result in a new signal flow driven circuit analysis and partition technique which is not anticipated, rendered obvious, suggested, or even implied by any of the prior art circuit analysis and partition, either alone or in any combination thereof.

To attain this, the present invention generally comprises automatic partition of mixed signal integrated circuits based on functional blocks, automatic identification of critical signal path in analog/RF circuits, automatic identification of fundamental unit circuits, automatic identification of matching and symmetry requirement. Circuit partition automatically partitions a mixed signal circuit into blocks based on their functionality. Identification of signal flow is achieved by automatically tracing the signal flow and identification of the critical path is based on a set of rules. Various building blocks of known characteristics and optimization requirement can also be automatically obtained. By tracing the signal path, matching and symmetry requirement and parasitic loading requirement at critical circuit nodes can also be automatically generated.

There has thus been outlined, rather broadly, the more important features of the invention in order that the detailed description thereof may be better understood, and in order that the present contribution to the art may be better appreciated. There are additional features of the invention that will be described hereinafter.

In this respect, before explaining at least one embodiment of the invention in detail, it is to be understood that the invention is not limited in its application to the details of construction and to the arrangements of the components set forth in the following description or illustrated in the drawings. The invention is capable of other embodiments and of being practiced and carried out in various ways. Also, it is to be understood that the phraseology and terminology employed herein are for the purpose of the description and should not be regarded as limiting.

A primary object of the present invention is to provide a signal flow driven circuit analysis and partition technique that will overcome the shortcomings of the prior art devices.

An object of the present invention is to provide a signal flow driven circuit analysis method by tracing signal flow.

An object of the present invention is to provide automatic circuit partition technique based on functionality and criticality.

An object of the present invention is to provide automatic circuit analysis to identify critical nodes, critical nets, critical components for performance assessment, yield enhancement, layout constrains generation, and circuit physical layout floor planning.

An object of the present invention is to provide a signal flow driven circuit analysis and partition technique for mixed signal circuit performance optimization, yield enhancement and layout optimization.

Another object is to provide a signal flow driven circuit analysis and partition technique that automatically identifies the critical signal path in the RF/Analog integrated circuits.

Another object is to provide a signal flow driven circuit analysis and partition technique that automatically identifies fundamental circuit units such as current mirrors, differential pairs, voltage or current references and stages of amplifiers etc.

Another object is to provide a signal flow driven circuit analysis and partition technique that automatically partitions a mixed signal circuit into digital (logic) section and analog/RF section.

Another object is to provide a signal flow driven circuit analysis and partition technique that automatically identifies matching devices and symmetry requirement for layout purposes.

Another object is to provide a signal flow driven circuit analysis and partition technique that automatically partition the analog/RF circuit section to critical signal path section and biasing circuit section for layout and/or circuit optimization purposes.

Other objects and advantages of the present invention will become obvious to the reader and it is intended that these objects and advantages within the scope of the present invention.

To the accomplishment of the above and related objects, this invention may be embodied in the form illustrated in the accompanying drawings, attention being called to the fact, however, that the drawings are illustrative only, and that changes may be made in the specific construction illustrated.

BRIEF DESCRIPTION OF THE DRAWINGS

Various other objects, features and attendant advantages of the present invention will become fully appreciated as the same becomes better understood when considered in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the several views, and wherein:

Fig.1 -- Signal Flow Driven Circuit Analysis and Partition Flow Chart

Fig.2 -- Means of Circuit Performance Assessment and Circuit Yield Enhancement Flow Chart

Fig.3 -- Means of Circuit Hierarchy Regeneration, Performance Optimization, Physical Layout Optimization, floor Planning, and Extracting Intellectual Property Circuit Cell Flow Chart

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning now descriptively to the drawings, in which similar reference characters denote similar elements throughout the several views, the attached figures illustrate a signal flow driven circuit analysis and partition technique, which comprises automatic partition of mixed signal integrated circuits based on functional blocks, automatic identification of critical signal path in analog/RF circuits, automatic identification of fundamental unit circuits, automatic identification of matching and symmetry requirement.
Circuit partition automatically partitions a mixed signal circuit into blocks based on their functionality. Identification of signal flow is achieved by automatically tracing the signal flow and identifies the critical path based a set of rules. Various building blocks of known characteristics and optimization requirement can also be automatically obtained. By tracing the signal path, matching and symmetry requirement and parasitic loading requirement at critical circuit nodes can also be automatically generated.

Circuit partition automatically partitions a mixed signal circuit into blocks based on their functionality. Circuit partition is performed by tracing the input/output signals of the circuit according to a set of "tracing rules": if a digital (analog) signal presents at the GATE of a MOSFET, then the SOURCE and DRAIN of this transistor is a digital (analog) node, unless it is terminated to supply rails (VCC or GND), denoted as: GATE -> SOURCE/DRAIN. We thus have: SOURCE-> DRAIN, DRAIN -> SOURCE, but not SOURCE or DRAIN -> GATE. On the other hand: resistors are transparent for both digital and analog signals, capacitors are transparent for analog signals but are open for digital, and inductors are mostly used as tuning load in RF circuits and rarely found in

digital integrated circuits. Upon finishing of the tracing, circuit partition is obtained. Circuit partition rules can be changed to accommodate other circuit topologies or requirement.

Identification of signal flow is achieved by automatically tracing the signal flow and identifies the critical path based a set of rules. The signal flow trackers does trace signal paths in RF/analog bock based on the rules: source to drain, drain to source, gate to drain, gate to source, but not drain to gate, not source to gate, and the termination is PWR/GND pin and other signal pins. Critical signal path is thus identified as those related to the critical input and/or output pins. With modified tracing rules, other circuit topologies can be accommodated.

Various building blocks of known characteristics and optimization requirement can also be automatically obtained. Automatically identifies the fundamental unit circuit based on structure representation by signal flow analysis, unit circuits include, but not limited to, various configurations of single stage amplifiers, current mirrors, differential pairs and voltage and current references. Unit circuit identification can also be achieved with pattern matching. Unit circuit can be expanded to some more complex sub-circuits.

By tracing the signal path, matching and symmetry requirement and parasitic loading requirement at critical circuit nodes can also be automatically generated. Automatically generates physical constraints such as matching, abutment and parasitic loading by a set of rule files as defined in the operation descriptions. It is possible to perform some simple numerical circuit simulation to enhance the constraints generation.

All components in this invention can be performed in series or in parallel. Depending on the application, they each can be performed separately if so desired: signal flow tracing and circuit partition in a numerical simulator, signal flow tracing and circuit partition in a circuit synthesizer, stand-alone signal flow driven circuit partition tool.

A signal flow tracker starts from the input terminals, and traces the signals as the following: For MOSFET, gate --> drain / source, drain --> source, source --> drain; for resistor, one terminal --> another terminal; for capacitor and inductor, same as for resistor; the terminations of signal path is PWR/GND or output ports. The unit circuit explorer works in two steps: first, unit circuit characterized structure generator produces the characteristic structure information, and the structure explorer search the matched structures for specified unit circuit. The matching explorer has three modules, differential pair explorer, current source explorer, and signal-path matching explorer. The differential pair explorer tries to find the differential pair based on the differential signal path. The two sides of differential pair must be matched. The current source explorer searches for the current sources and current mirrors, where the matched transistors are identified. The signal path matching explorer searches for matched signal flow paths based on the signal flow tracing.

The non-critical device explorer has three modules, the logic signal tracker, the logic-driven-gate MOS explorer, and the capacitor-connected MOS explorer. The logic signal flow tracker traces the logic according to the given rules. The logic-driven-gate MOS explorer searches the MOSFETs whose gates are driven by the logic signals. The capacitor-connected MOS explorer searches for the MOSFETs connected as capacitors.

The bias circuit explorer has four modules, the unit circuit explorer, matching explorer, not critical device explorer, and the bias circuit re-builder. The unit circuit explorer tries to dig out all the unit circuits, to make the bias circuit hierarchy. Matching explorer tries to dig out the matching in the bias circuit. The not critical device explorer tries to dig out all the not critical devices in the bias circuit. The bias circuit re-builder tries to re-build the bias circuit with the identified unit circuit as a sub-circuit.

In the core circuit explorer, the signal flow tracker tries to separate the signal path for each critical signal; the zipper cell explorer tries to dig out the common part of the two or more signal paths, the signal path matching explorer tries to dig out the matching between two signal paths, the unit circuit explorer tries to dig out the unit circuits in the

core circuit, the core circuit re-builder tries to re-build the core circuit, with the zipper cell as a sub-circuit, the un-shared part of the signal path as a sub-circuit, the unit circuit of the signal path regarded as the sub-circuit in the signal path sub-circuit, so that the core circuit is re-organized as a hierarchy circuit.

In the logic and analog/RF explorer, the signal flow tracker spread the logic signals or analog/RF signals from the input based on the given rules; the devices with all terminals driven by logic signal are partitioned into logic circuits. Others are classified into the analog/RF circuit. The logic circuit builder tries to build the logic sub-circuit; the analog circuit builder tries to build the analog/RF sub-circuit; and the whole circuit reorganized as the instantiation of the logic sub-circuit and the analog/RF sub-circuit. The logic sub-circuit will further handled by logic circuit explorer that is out of this invention.

The analog/RF circuit will be further handled by bias and core circuit partitioner. The bias and core circuit partitioner tries to partition the analog/RF circuit into bias circuit and core circuit based on the critical signal tracing. The analog/RF circuit re-organized as the instantiations of bias sub-circuit and core sub-circuit. The bias sub-circuit will be further handled by the bias circuit explorer and the core sub-circuit will be further handled by the core circuit explorer. Therefore, a circuit will be re-organized as a new hierarchy circuit with logic and analog/RF partitioned, bias and core partitioned, signal path partitioned, unit circuit identified, symmetry and matching identified, etc., which will be potentially used for speeding up circuit simulation, circuit optimization, yield improvement, efficiently controlling layout synthesis, circuit physical layout floor panning, and extracting Intellectual Property circuit cell for reuse, etc.

As to a further discussion of the manner of usage and operation of the present invention, the same should be apparent from the above description. Accordingly, no further discussion relating to the manner of usage and operation will be provided.

With respect to the above description then, it is to be realized that the optimum dimensional relationships for the parts of the invention, to include variations in size,

materials, shape, form, function and manner of operation, assembly and use, are deemed readily apparent and obvious to one skilled in the art, and all equivalent relationships to those illustrated in the drawings and described in the specification are intended to be encompassed by the present invention.

Therefore, the foregoing is considered as illustrative only of the principles of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation shown and described, and accordingly, all suitable modifications and equivalents may be resorted to, falling within the scope of the invention.